REMARKS

This responds to the Office Action mailed on April 5, 2007.

Claims 1-5, 9-14 and 19-23 are amended, claims 7, 8 and 15-18 are canceled, and claims 24-29 are added; as a result, claims 1-6, 9-14 and 19-29 are now pending in this application.

Drawings

A complete set of replacement formal drawings (Figs. 1A-5) is filed herewith.

Claim Objections

Claims 19 and 22 were objected to for informalities. Specifically, the Examiner points out that the limitations "queueing" in line 2 of claim 19 and "inserting to first" in line 2 of claim 22 should instead read "queuing" and "inserting to the first," respectively.

Claims 19 and 22 have been amended to more clearly define Applicant's claimed invention as requested by the Examiner.

§112 Rejection of the Claims

Claims 1-23 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Specifically, the Examiner points out that the limitation "one or memory requests" in claims 1, 11 and 21 is vague. The Examiner also points out that the limitation "the first synchronization instruction" in claims 3, 4, 13, 14 and 23 lacks sufficient antecedent basis in the claims.

Claims 1, 3, 4, 11, 13, 14, 21 and 23 have been amended to more clearly define Applicant's claimed invention as requested by the Examiner.

§102 Rejection of the Claims

Claims 1, 11 and 21 were rejected under 35 U.S.C. § 102(b) for anticipation by Smith et al. (US 2002/0116600).

Applicant's invention as claimed in amended claims 1, 11 and 21, pertains to a method and apparatus for memory synchronization. Specifically, Applicant's memory synchronization deals with how to take the outcomes of the execution of instructions by a plurality of processing units and to commit those outcomes to memory in a deterministic order regardless of the order of

the execution of the instructions by the processing units. To achieve this, Applicant's invention claims in amended claims 1, 11 and 21, using a first plurality of queues connected to a memory interface for holding memory requests. In addition, Applicant further claims in amended claims 1, 11 and 21, that the memory requests are memory references generated as a result of execution of instructions by one or more instruction-processing circuits.

Smith describes a method and apparatus for instruction synchronization. Although the instruction synchronization in Smith deals with how to execute and retire instructions in a processing unit in a program order, Smith does not teach or suggest the memory synchronization method and apparatus as taught by Applicant and claimed in amended claims 1, 11 and 21.

For example, first of all, the reorder buffer (Fig. 6A, 162) under Smith's approach is connected to the execution unit (Fig. 2, 70) of a microprocessor. This makes sense because the reorder buffer is used to store microinstructions and to retire them in a program order as the microinstructions are executed by the execution unit (e.g., [0053], lines 19-27). In contrast, Applicant's queues are connected to a memory interface. This difference also makes sense because Applicant's memory synchronization deals with the order in which the outcomes of execution of instructions are further processed (e.g., committed) into a memory as discussed above. That is, Smith is trying to ensure that instructions execute in a particular order. Applicant, on the other hand, is trying to prevent a race condition from developing when reading and writing to the same memory address from two or more memory queues.

In addition, as discussed above, the microinstructions stored in the reorder buffer under Smith's approach are instructions to be executed by the execution unit. In contrast, the memory requests under Applicant's approach are memory references resulting from execution of instructions by the instruction-processing circuits. Applicant is unable to find these teachings in Smith. Claims 1, 11 and 21 have been amended to emphasize these differences.

The newly added limitations are fully supported from Applicant's original Specification. For example, as noted at Fig. 1L & 2, p. 58, lines 3-29 and p. 66, lines 9-29, Applicant teaches that Vector Request Port Queues (VRQs: Fig. 1L, 161, 162, 163), Vector Data Queues (VDQs: Fig. 1L, 171, 172, 173) and Scalar Queues (SQs: Fig. 1L: 181, 182, 183) are located in E-chip Interface Unit (EIU: Fig. 1L, 116). Applicant further teaches that the EIU (116) is connected to E-chips (Figs. 1L & 2: 101), which in turn are connected to Memory (Fig. 2: 105).

Applicant also teaches that: the VRQs (161-163) contain vector load or store addresses generated by Vector Load/Store Unit (111) (p. 58, lines 3-6); the VDQs (171-173) contain vector store data generated by Vector Unit (113) (Fig. 1L, p. 36, line 15 through p. 37, line 12 and p. 58, lines 10-18); and the SQs (181-183) contain scalar addresses and scalar store data that have been sent from Scalar Unit (134) (id. lines 19-21). Reconsideration is respectfully requested.

§103 Rejection of the Claims

Claims 2-6, 9, 10, 12-16, 19, 20, 22 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Chen et al. (US 5,197,130).

Smith is discussed above.

Chen describes cluster architecture for a highly parallel scalar/vector multiprocessor system. Specifically, Chen describes using dedicated scalar registers and vector registers (Fig. 4, 64, 16).

Claims 2, 12 and 22 are patentable as being dependent on a patentable base claim. In addition, neither Smith nor Chen, alone or in combination, teach or suggest using dedicated queues for vector memory requests and scalar memory requests, respectively for memory synchronization purpose as taught by Applicant and claimed in claims 2, 12 and 22.

Although Chen describes using the dedicated registers, they are designed to temporarily store outcomes (or memory references thereof) resulting from execution of corresponding vector or scalar instructions. Chen does not, however, teach or suggest using the registers for controlling the order in which the resulting memory references are processed into a memory. Reconsideration is respectfully requested.

Claims 3-6, 9, 10, 13-16, 19, 20 and 23 are patentable as being dependent on a patentable base claim.

Claims 7-8 and 17-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Barnes et al. (US 4,412,303).

Smith is discussed above.

Barnes describes array processor architecture. Barnes also describes a method and apparatus for synchronizing instructions (commands) from given processors. For example, the

Connection Network Buffer (CN BUFF) (23) is connected to a corresponding procedure rather than to a memory interface. See Figs. 1 & 2 and col. 6, lines 19-31. Also, the Coordinator (21) controls execution of instructions (e.g., 'halt' the processor or 'release' its halt commands through lines 31 and 33 and all processors (29) begin in parallel to execution of the next task or instruction). *Id.*

Claims 7, 8, 17 and 18 have been canceled. New claims 24-29 have been added. New claims 24 and 27 are fully supported from Applicant's original Specification. For example, as noted at Figs. 1L & 2, p. 68, lines 1-11 and original claims 8 and 18, Applicant teaches using Lsync instructions and Msync instruction together to provide hierarchical memory ordering not only for a local processor but also for a plurality of processors. New claims 25 and 28 are supported, for example, by Fig. 2, block 248. New claims 26 and 29 are supported, for example, by Applicant's original claims 10 and 20, respectively.

New claims 24 and 27 are patentable for the similar reasons as noted in the discussion of claims 1, 11 and 21. In addition, new claims 24 and 27 are patentable since neither Smith nor Barnes, alone or in combination, teach or suggest using Lsync instructions and Msync instructions together to support memory ordering for a plurality of processors as discussed above. New claims 25, 26, 28 and 29 are patentable as being dependent on a patentable base claim. Allowance of theses new claims is respectfully requested.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence

of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date June 4, 2007

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 4 day of June 2007.

CANDIS BUENDING

Name

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